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Combatting latency and packet jitter in packet switched networks

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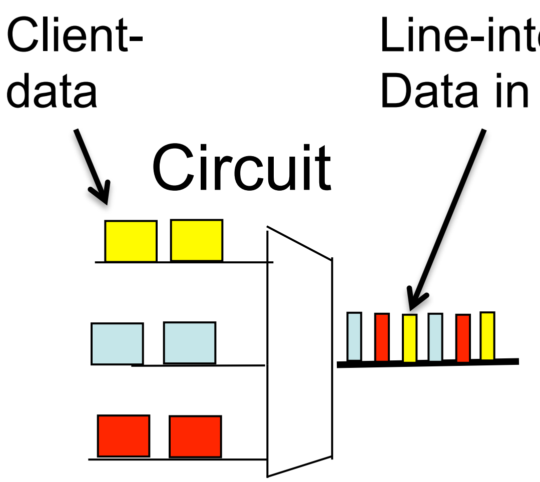
Outline

- Circuit and packet switched networks comparison
  - Sources of packet jitter
- Latency and packet jitter (Packet delay variation)
  - Sources in packet networks
  - How to combat packet jitter
- Summary and some thought on framing

Circuit versus packet switching

- Circuit: Static multiplexing
  - Deterministic scheduling
  - Client interface data multiplexed into predictable fixed time-slots on line-interface
  - Line interface capacity > = sum of client interface capacities

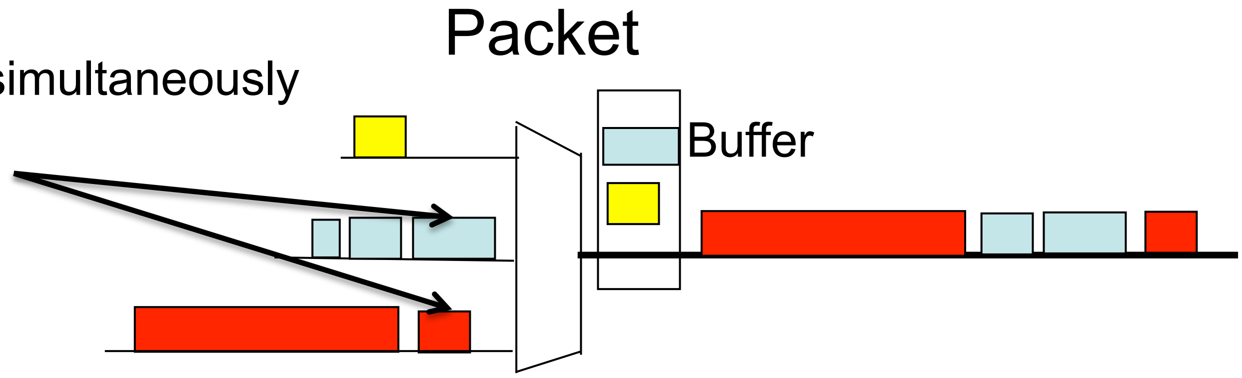


Fixed length frames
Dedicated time-slots
Static multiplexing
Ultra-low packet-jitter

Circuit versus packet switching

- Packet: Statistical multiplexing = non deterministic
  - Line-interface capacity may be lower than sum of client-interface capacities.
  - Packets of variable size
  - Statistical arrival

Two packets arriving at client simultaneously heading for the same output.

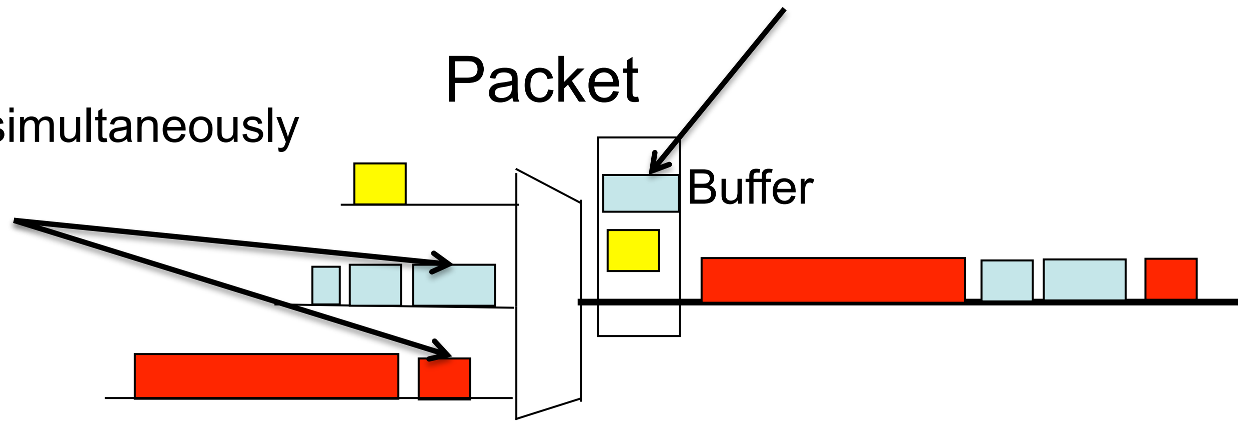


Circuit versus packet switching

- Packet: Statistical multiplexing = non deterministic
  - Line-interface capacity may be lower than sum of client-interface capacities.
  - Packets of variable size
  - Statistical arrival

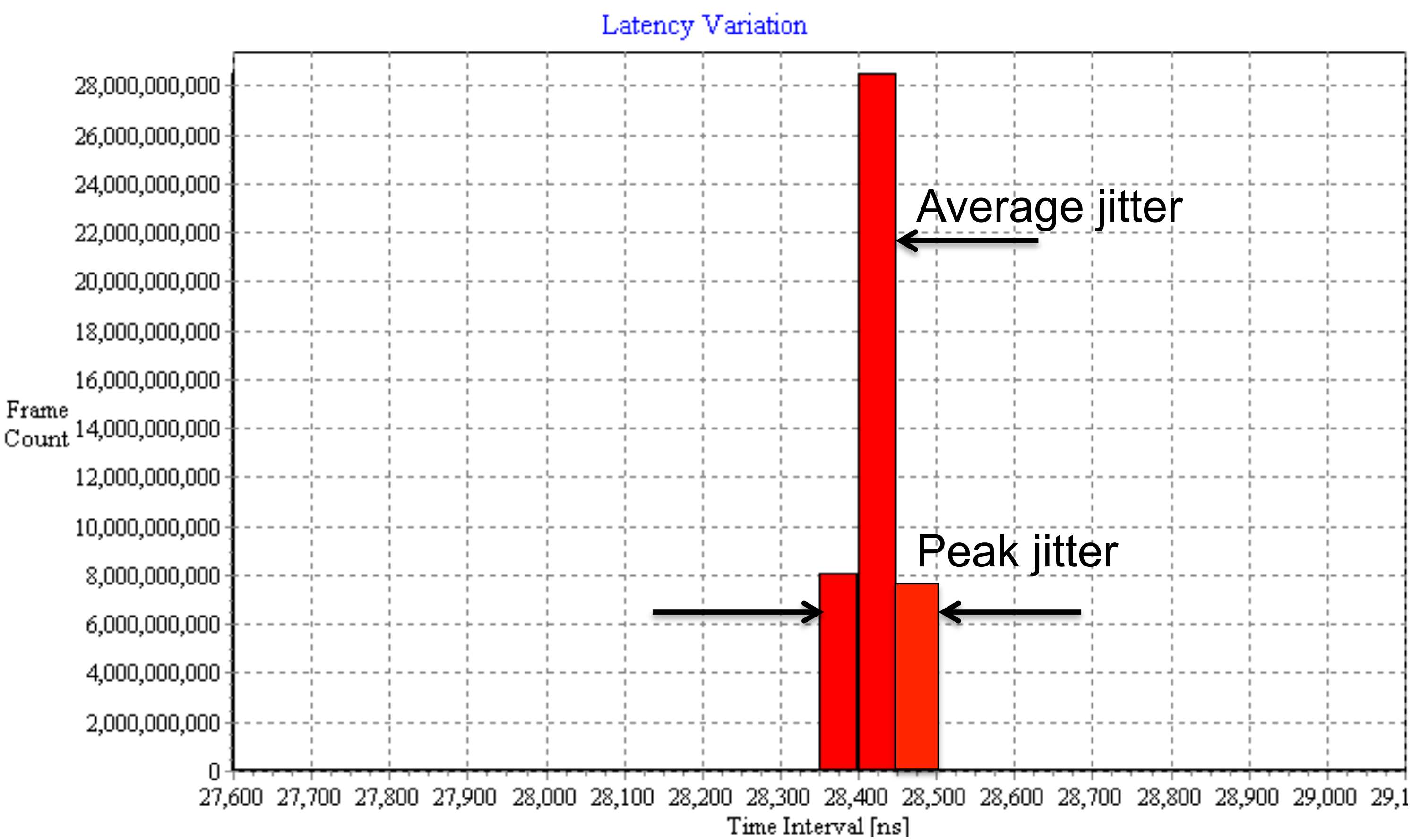
One packet must wait in the buffer.
Waiting time depends on packet length
Variable waiting time implies packet jitter

Two packets arriving at client simultaneously heading for the same output.



Packet-jitter distribution example

- How is jitter measured
  - Peak jitter (maximum): Slowest – fastest
  - Average jitter: The average value of packet arrivals



Packet-jitter and latency demands

- Mobile backhaul
  - Using IEEE1588 for synchronization
  - Average jitter important to keep low
  - Sync. Accuracy in the microsecond range
- Mobile fronthaul - CPRI over Ethernet
  - Peter Ashwood Smith, IEEE 802, July 2014:

REQUIRED

- 100us – Maximum one way Delay between Antenna and Compute
- 65ns – Maximum variation in Delay (Jitter).
- 1-10G – Throughput per antenna (compression possible).
- 10-12 – Maximum Bit Error Rate

OBSERVED

Average latency = 3us per hop

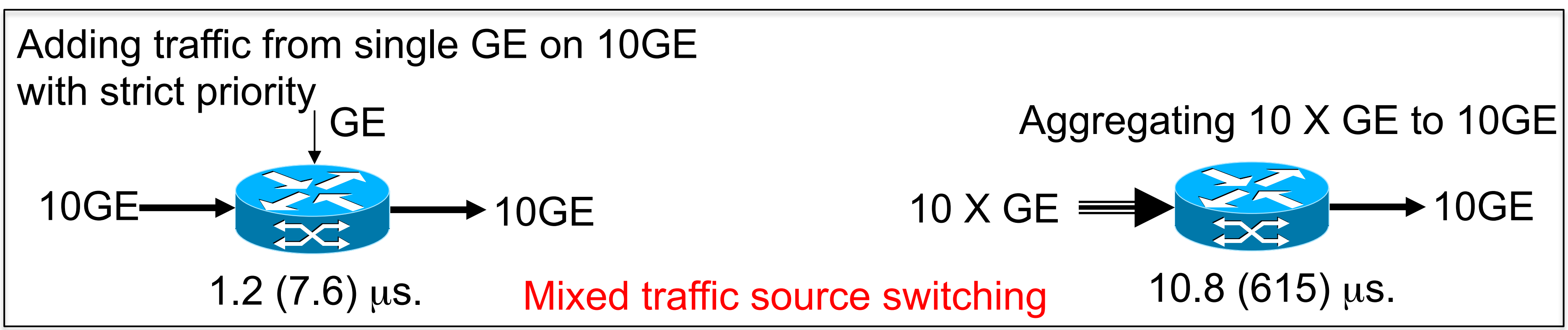
Peak Jitter = +/- 2500ns per hop

Packet-jitter and latency sources

- Circuit (OTN/SDH)
  - Clock domain conversion
  - Depends on design
  - Typically < 10 ns at 10 Gb/s
- Packet
  - Clock domain conversion, typ. < 10 ns at 10 Gb/s
  - Header processing (may be fixed)
  - Contention and buffering
    - Microseconds/milliseconds
    - Jitter depends on traffic-load

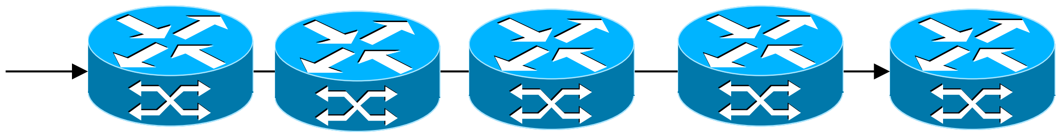
Packet-jitter sources in packet switching

- Minimum peak values through single node
- 1518 Byte frames (9600 B Jumbo-Frames)
- Requirement: 65 ns



Performance degrades through a network with many hops

- Contribution from each hop (switch, router)
- Packet loss and latency adds up
  - N nodes of PLR = 1 X 10^-5 => PLR = N X 10^-5



- Peak PDV adds up while mean PDV depends on PDV distribution of each node

How to combat Packet-jitter

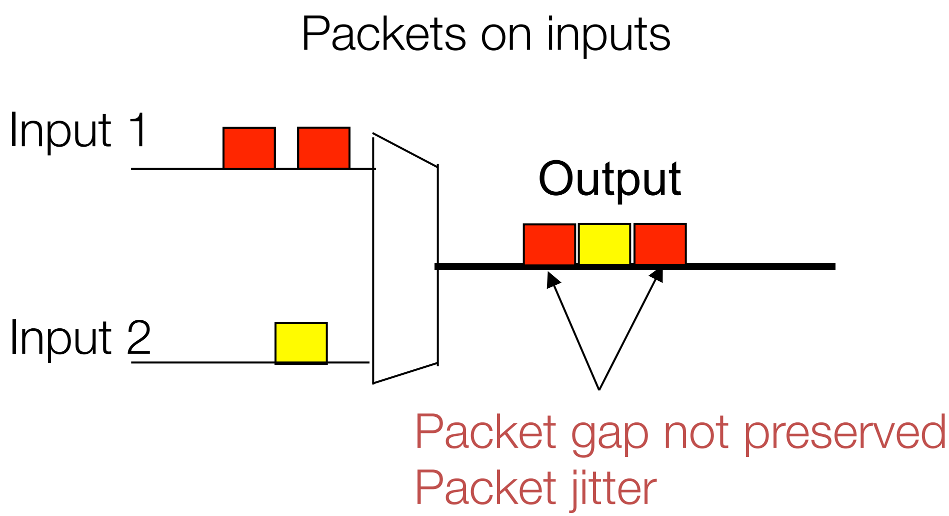
- Aggregating traffic
  - Deterministic scheduling similar to TDM
  - May schedule packets into virtual time-slots
  - Proprietary method of aggregation
- Mixing traffic
  - Absolute priority QoS separation mechanism
  - CPRI traffic receives absolute priority
  - Proprietary method for QoS separation

Combatting packet jitter

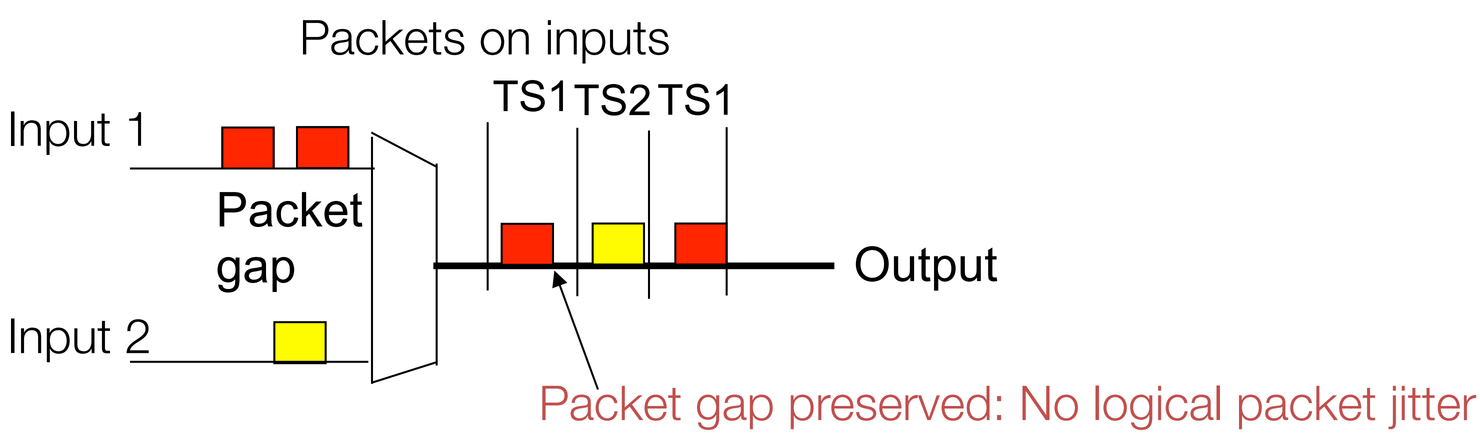
- Integrated hybrid optical network (IHON)
  - Combining circuit and packet switching techniques
  - Still pure packet based, no TDM
  - Properties from Circuit and Packet networks combined
- FUSION networks
  - IHON known from academic literature: Published in major IEEE conferences and journals
  - Not standardized
  - Commercialized as FUSION networks (TransPacket)

Packet versus Fusion aggregation

- Packet aggregation

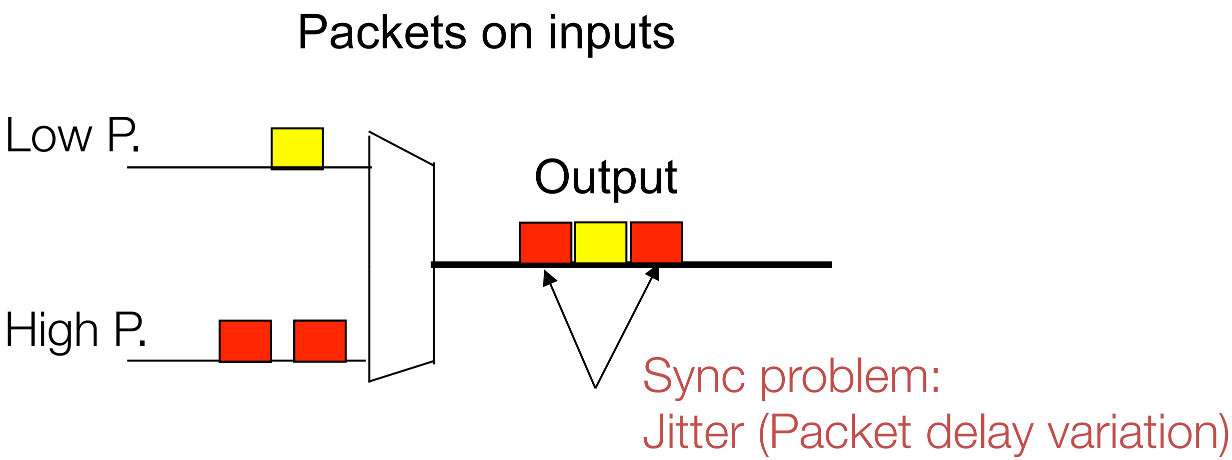


- Fusion deterministic aggregation: Virtual Time-slots

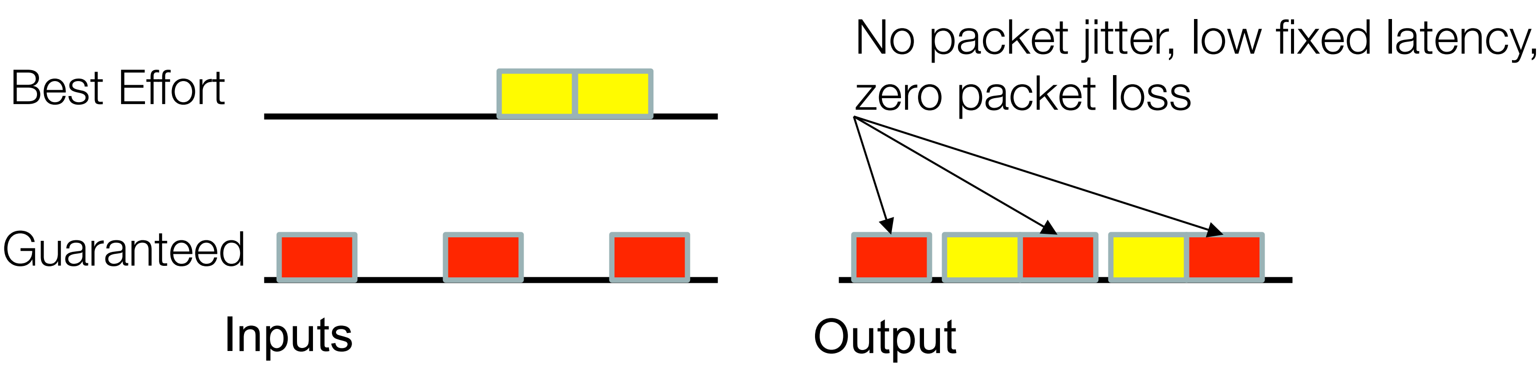


Packet versus Fusion absolute priority

- Traditional QoS scheduling introduce jitter (strict priority)

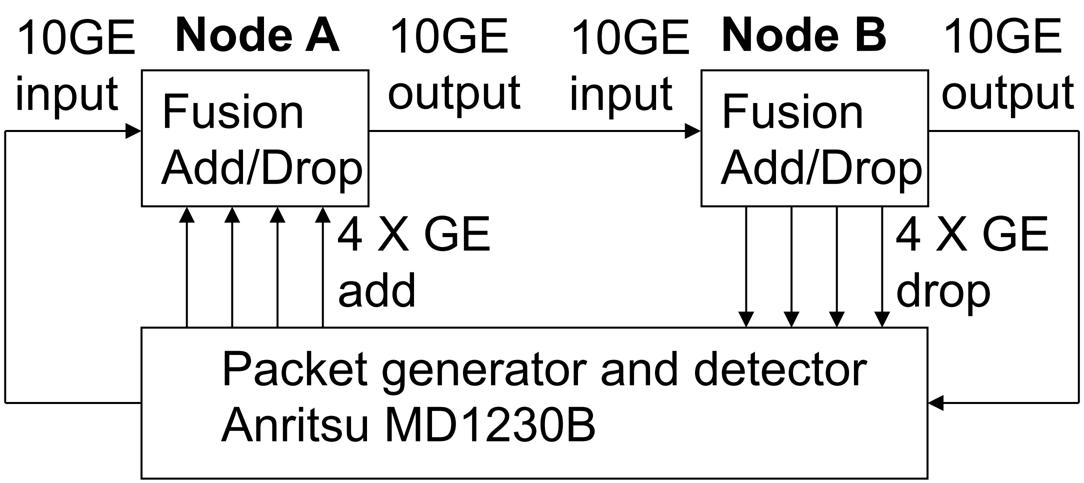


- Fusion absolute priority scheduling: No jitter



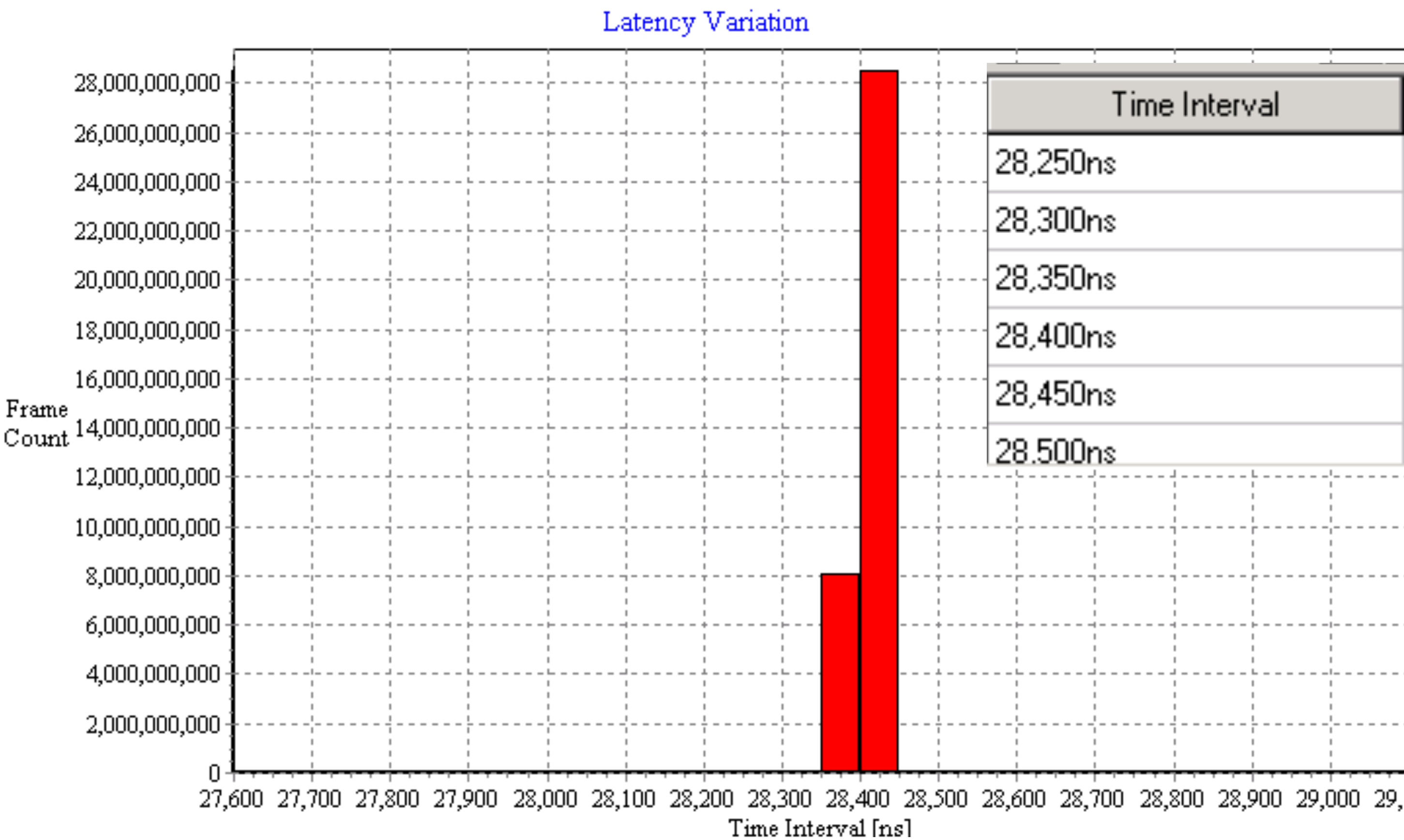
Experiment on absolute priority

- Setup emulating GE traffic added to 10GE
- 10GE traffic receives absolute priority



Experimental results

- Packet-jitter approximately 50 ns
  - Requirement 65 ns
- Resolution on tester is too low for high accuracy



Time Interval	Frame Count
28,250ns	0
28,300ns	0
28,350ns	8,122,524,200
28,400ns	28,626,174,822
28,450ns	0
28,500ns	0

Achievable latency/packet jitter

- Aggregating traffic
  - Logical contribution is zero jitter
  - Current implementation is approx. 400 ns
  - Latency depends on maximum length (MTU) on guaranteed frames.
- Mixing traffic
  - Logical jitter is zero, current implementation approx. 50 ns.
  - Absolute priority traffic fixed delay according to MTU on lower priority frames. (e.g. 1.2 us @ 10 Gb/s for MTU = 1518 Bytes)
  - Additional delay contribution from processing etc.

Summary/Thoughts on framing

- Conventional packet switches main challenge is packet jitter
  - Packet jitter increases with increasing load and number of hops.
- IHON/FUSION
  - Less than 65 ns packet jitter is achievable
  - Load independent.
- CPRI framing: Short packets lowers latency
  - Benefits from lower serialization delay
  - Lowers aggregation delays in IHON/FUSION
  - Increases overhead on framing

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FUSION NETWORKS